What is Claimed is:

[c1] A method for reducing shorts in an integrated circuit design having cells, said method comprising:

identifying faulty vias as ones having a chance of shorting that is above a predetermined threshold;

evaluating an original cell containing a faulty via to determine if a redundant via exists for said faulty via; and

removing said faulty via from said original cell to create a cloned cell.

[c2] The method of claim 1, wherein said method further comprises replacing said original cell with said cloned cell in said integrated circuit design.

[c3] The method of claim 1, wherein said identifying comprises selecting vias that violate predetermined spacing tolerances.

[c4] The method of claim 1, wherein said method further comprises:

locating a cluster of vias in said integrated circuit design; and

associating faulty vias and redundant vias in said cluster.

[c5] The method of claim 1, wherein said identifying comprises locating pairs of potentially shorting vias, wherein potentially shorting vias comprise a pair when a probability that a short will occur between said potentially shorting vias exceeds a predetermined threshold.

[c6] The method of claim 1, wherein said method further comprises building a layout design utilizing said cloned cell.

[c7] The method of claim 1, wherein said method further comprises:

identifying a first potentially shorting via and a second potentially shorting via; and

evaluating whether it is more efficient to remove said first potentially shorting via or said second potentially shorting via.

[c8] A system for reducing shorts in an integrated circuit design having cells, said system comprising:

an identifier for identifying faulty vias as ones having a chance of shorting

that is above a predetermined threshold;

an evaluator for evaluating an original cell containing a faulty via to determine if a redundant via exists for said faulty via; and

a remover for removing said faulty via from said original cell to create a cloned cell.

[c9] The system of claim 8, wherein said system further comprises a replicator for replacing said original cell with said cloned cell in said integrated circuit design.

[c10] The system of claim 8, wherein said system further comprises a locator for locating a cluster of vias in said integrated circuit design; and

wherein said identifier associates faulty vias and redundant vias in said cluster.

[c11] The system of claim 8, wherein said system further comprises a user interface for applying said cloned cell to said integrated circuit design.

[c12] The system of claim 8, wherein said system further comprises a builder for building a layout design utilizing said cloned cell.

[c13] The system of claim 8, wherein said system further comprises a tester for testing said layout design.

[c14] The system of claim 8, wherein said system further comprises:

an identifier for identifying a first potentially shorting via and a second potentially shorting via; and

an evaluator for evaluating whether it is more efficient to remove said first potentially shorting via or said second potentially shorting via.

[c15]

A method for reducing shorts in an integrated circuit design having cells, said method comprising:

identifying faulty vias as ones having a chance of shorting that is above a predetermined threshold;

evaluating an original cell containing a faulty via to determine if a redundant via exists for said faulty via;

using said redundant via in place of said faulty via to create a cloned cell;

and

replacing said original cell with said cloned cell in said integrated circuit design.

[c16] The method of claim 15, wherein said identifying comprises selecting vias that violate predetermined spacing tolerances.

[c17] The method of claim 15, wherein said method further comprises:

locating a cluster of vias in said integrated circuit design; and

identifying faulty vias and associated redundant vias in said cluster.

[c18] The method of claim 15, wherein said identifying comprises locating pairs of potentially shorting vias, wherein potentially shorting vias comprise a pair when a probability that a short will occur between said potentially shorting vias exceed a predetermined threshold.

[c19] The method of claim 15, wherein said method further comprises building a layout design utilizing said cloned cell.

[c20] The method of claim 15, wherein said method further comprises:

identifying a first potentially shorting via and a second potentially shorting via; and

evaluating whether it is more efficient to remove said first potentially shorting via or said second potentially shorting via.

[c21] A program storage device readable by machine, tangibly embodying a program of instructions executable by said machine to perform a method for reducing shorts in an integrated circuit design having cells, said method comprising:

identifying faulty vias as ones having a chance of shorting that is above a predetermined threshold;

evaluating an original cell containing a faulty via to determine if a redundant via exists for said faulty via; and

removing said faulty via from said original cell to create a cloned cell.

[c22] The program storage device of claim 21, wherein said method further comprises replacing said original cell with said cloned cell in said integrated circuit design.

[c23] The program storage device of claim 21, wherein said identifying comprises selecting vias that violate predetermined spacing tolerances.

[c24] The program storage device of claim 21, wherein said method further comprises:

locating a cluster of vias in said integrated circuit design; and

associating faulty vias and redundant vias in said cluster.

[c25] The program storage device of claim 21, wherein said identifying comprises locating pairs of potentially shorting vias, wherein potentially shorting vias comprise a pair when a probability that a short will occur between said potentially shorting vias exceeds a predetermined threshold.

[c26] The program storage device of claim 21, wherein said method further comprises building a layout design utilizing said cloned cell.

[c27] The program storage device of claim 21, wherein said method further comprises:

identifying a first potentially shorting via and a second potentially shorting via; and

evaluating whether it is more efficient to remove said first potentially shorting via or said second potentially shorting via.